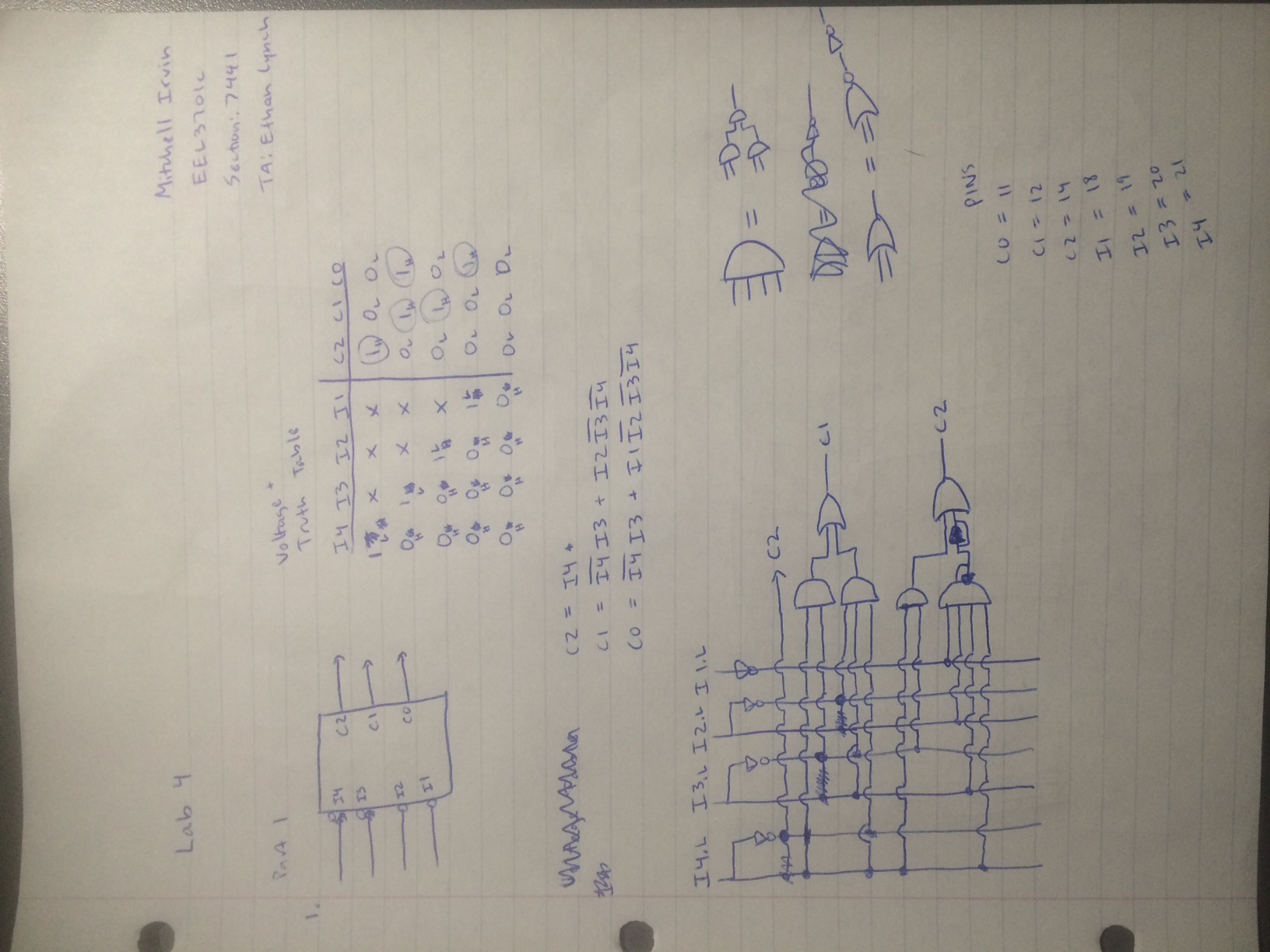
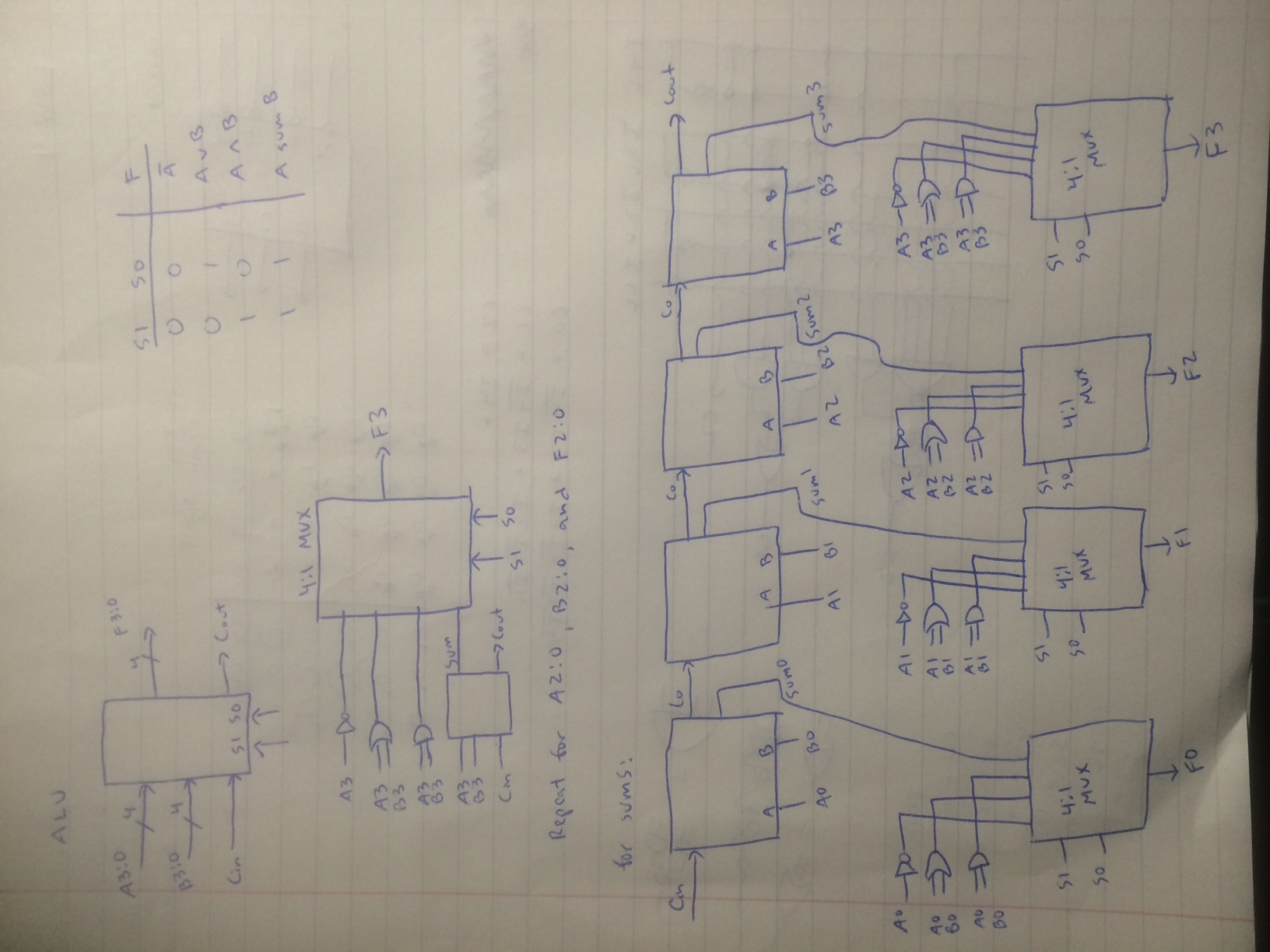
Lab 4 Summary

Irvin, Mitchell

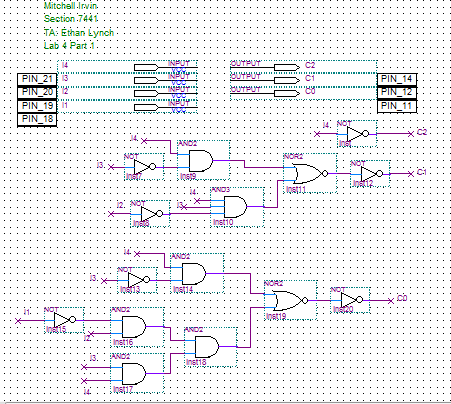
Section 7441

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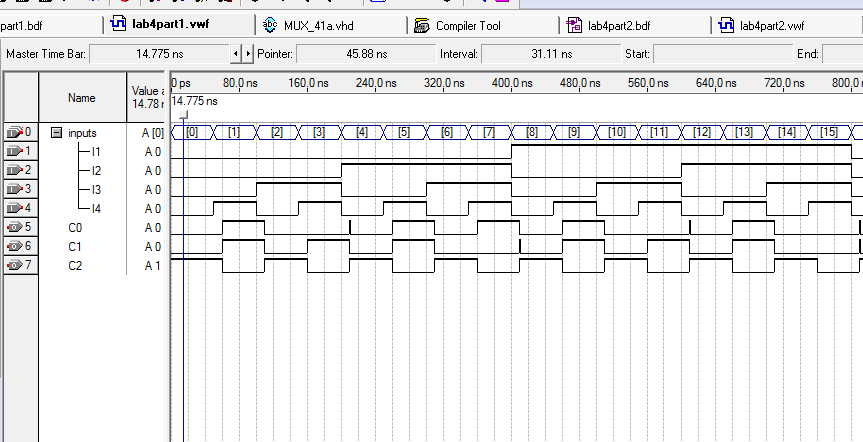




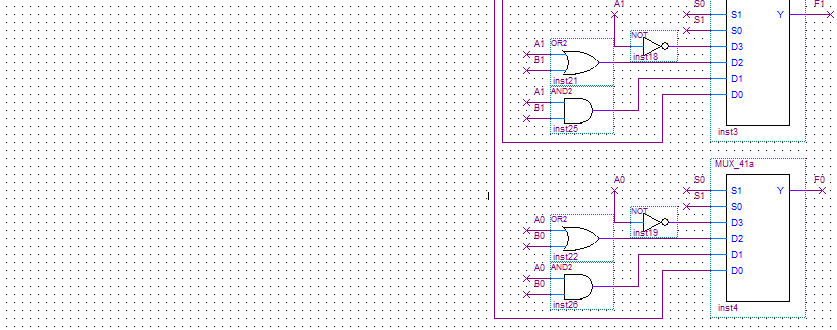
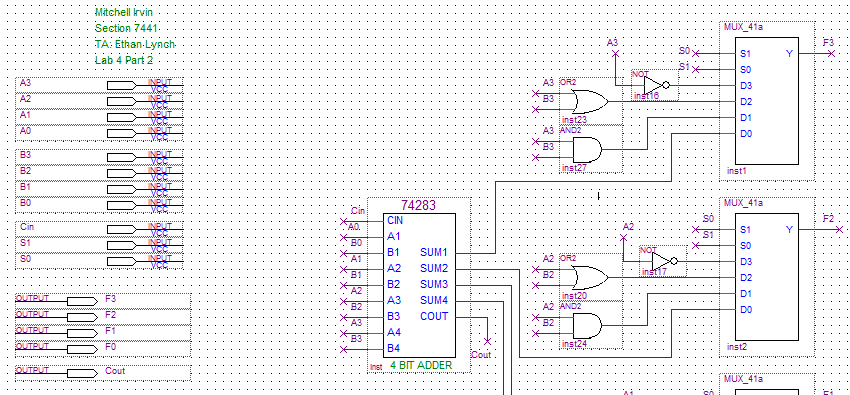
Part 1 BDF



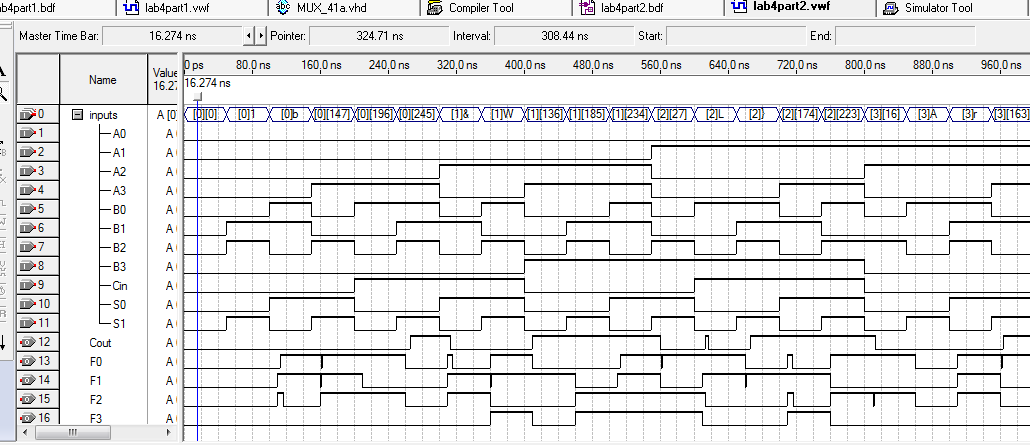
Part 1 VWF



Part 2 BDF



Part 2 VWF



4:1 MUX VHDL file

